



GAN7R0-150LBE

150 V, 7 mOhm Gallium Nitride (GaN) FET in a
2.2 mm x 3.2 mm x 0.774 mm Land Grid Array (LGA) package

24 April 2023

Product data sheet

1. General description

The GAN7R0-150LBE is a general purpose 150 V, 7 mΩ Gallium Nitride (GaN) FET in a Land Grid Array (LGA) package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Land Grid Array (LGA) package 2.2 mm x 3.2 mm x 0.774 mm

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, (secondary stage)
- High frequency DC-to-DC converters in 48 V systems
- 400 V to 48 V LLC converters, secondary (rectification) side
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- LiDAR (non-automotive)
- Class D audio amplifiers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	-	150	V
V_{TDS}	transient drain to source voltage	pulsed; $t_p = 1 \mu\text{s}$; $\delta_{\text{factor}} = 0.01$	-	-	170	V
I_D	drain current	$V_{GS} = 5 \text{ V}$	[1]	-	28	A
P_{tot}	total power dissipation	Fig. 1	-	-	28	W
T_j	junction temperature		-40	-	150	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}$; $I_D = 10 \text{ A}$; $T_j = 25 \text{ °C}$; Fig. 9 ; Fig. 10 ; Fig. 11 ; Fig. 12	-	5.6	7	mΩ
R_G	gate resistance	$f = 5 \text{ MHz}$; $T_j = 25 \text{ °C}$	-	2.3	-	Ω

150 V, 7 mOhm Gallium Nitride (GaN) FET in a 2.2 mm x 3.2 mm x 0.774 mm Land Grid Array (LGA) package

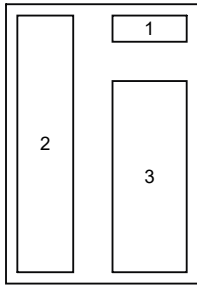
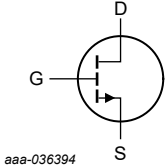
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 85\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13; Fig. 14	-	1.3	-	nC
$Q_{G(\text{tot})}$	total gate charge		-	7.6	-	nC
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 85\text{ V}$; $T_j = 25\text{ °C}$	[2]	47	-	nC

[1] Limited by package

[2] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view FCLGA3 (SOT8073-1)</p>	 <p>aaa-036394</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN7R0-150LBE	FCLGA3	flip chip land grid array package; no leads; body: 3.2 x 2.2 x 0.774 mm, 3-pad	SOT8073-1

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN7R0-150LBE	7R0ELBE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	150	V
V_{TDS}	transient drain to source voltage	pulsed; $t_p = 1\text{ }\mu\text{s}$; $\delta_{\text{factor}} = 0.01$	-	170	V
V_{GS}	gate-source voltage		-4	6	V

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Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	Fig. 1	-	28	W
I_D	drain current	$V_{GS} = 5\text{ V}$	[1]	28	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\ \mu\text{s}$; Fig. 2	[1]	120	A
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-40	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C

[1] Limited by package

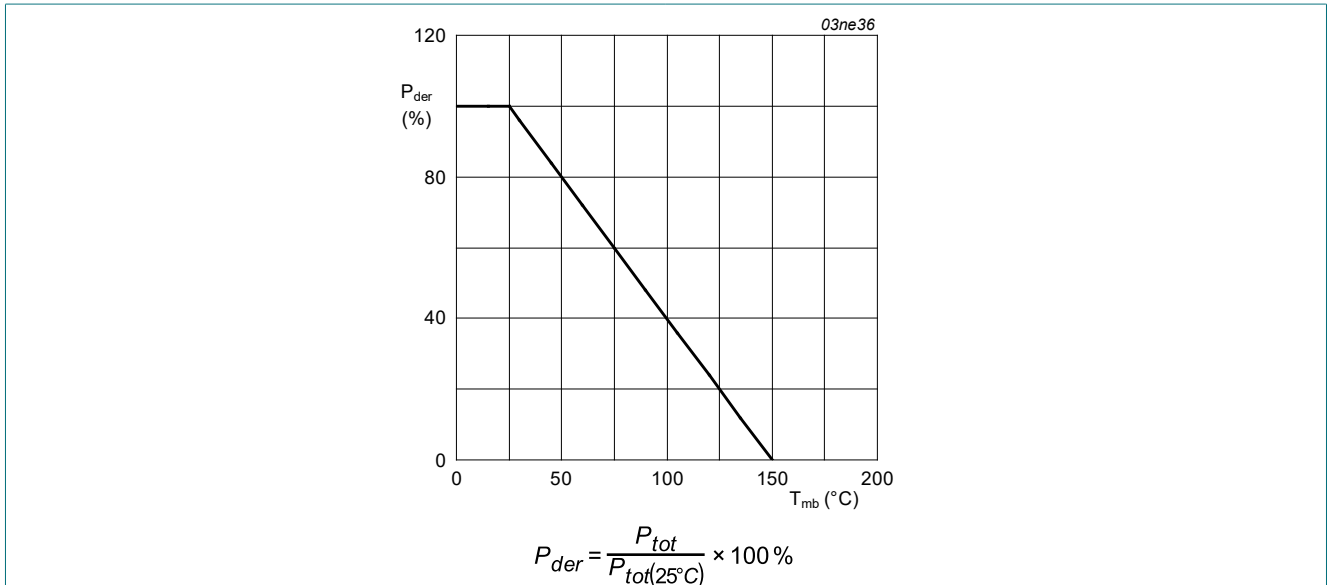


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

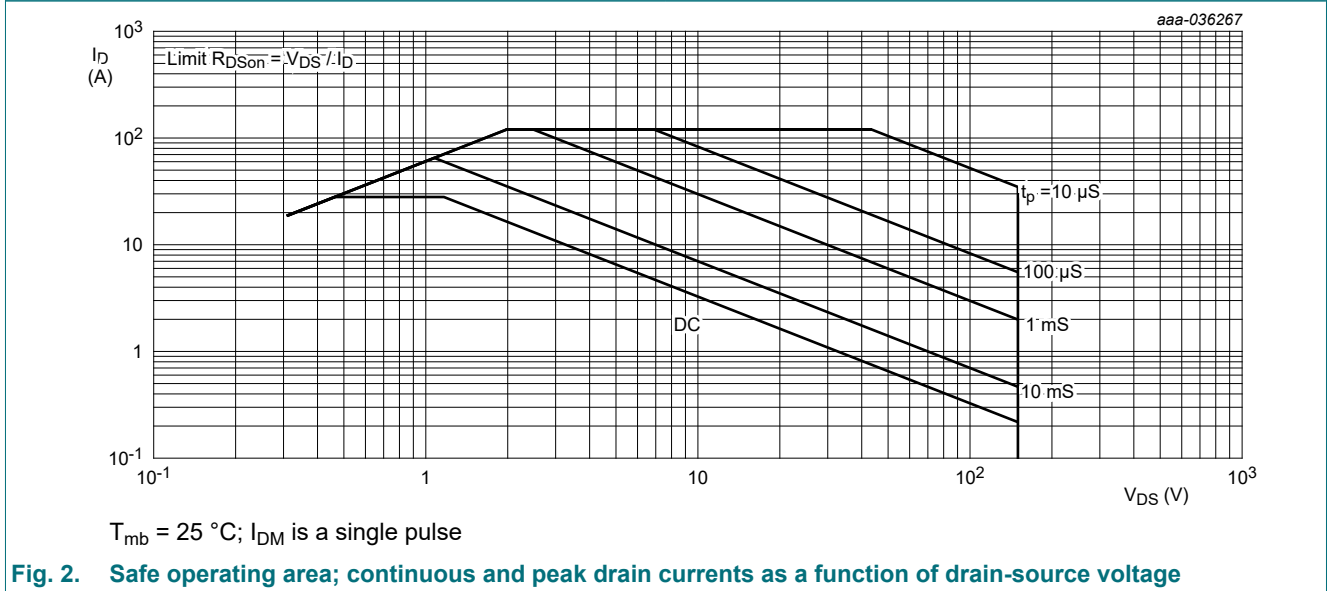


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		-	-	26	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3	-	-	4.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	-	57	K/W

[1] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

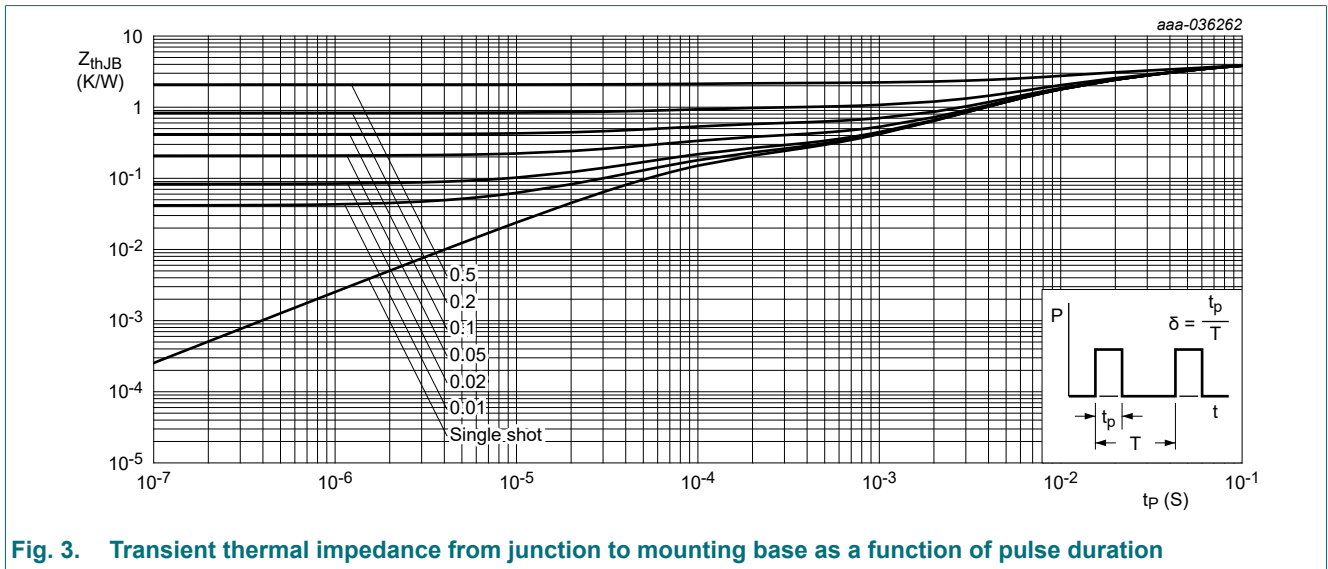


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

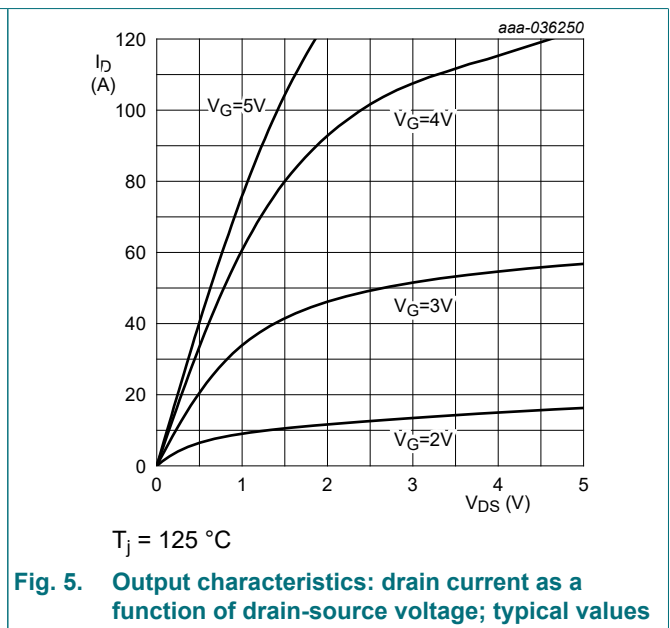
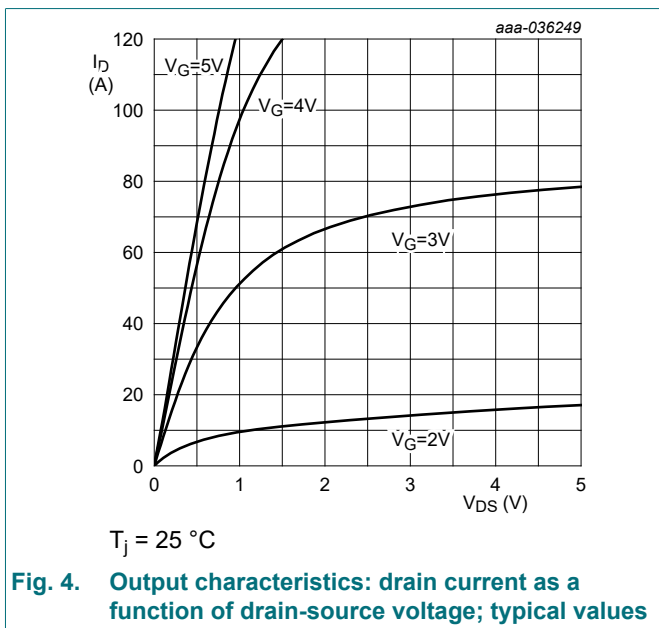
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 150 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 5 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 8}$	0.8	1.1	2.1	V
I_{DSS}	drain leakage current	$V_{DS} = 120 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	8	45	μA
I_{GSS}	gate leakage current	$V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$	-	1	32	μA
		$V_{GS} = -4 \text{ V}; T_j = 25 \text{ }^\circ C$	-	8	45	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}; \text{ Fig. 11}; \text{ Fig. 12}$	-	5.6	7	m Ω
R_G	gate resistance	$f = 5 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	2.3	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 85 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 13}; \text{ Fig. 14}$	-	7.6	-	nC
Q_{GS}	gate-source charge		-	1.7	-	nC
Q_{GD}	gate-drain charge		-	1.3	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 85\text{ V}; V_{GS} = 0\text{ V}; f = 100\text{ kHz};$	-	865	-	pF
C_{oss}	output capacitance	$T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	280	-	pF
C_{rss}	reverse transfer capacitance		-	2.5	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0\text{ V} \leq V_{DS} \leq 85\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16	[1]	380	-	pF
$C_{o(tr)}$	effective output capacitance, time related	$0\text{ V} \leq V_{DS} \leq 85\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 25\text{ }^\circ\text{C}$	[2]	555	-	pF
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 85\text{ V}; T_j = 25\text{ }^\circ\text{C}$	[3]	47	-	nC
Source-drain characteristics						
V_{SD}	source-drain voltage	$I_S = 0.5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17 ; Fig. 18 ; Fig. 19 ; Fig. 20	-	1.2	-	V

- [1] $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 85 V
- [2] $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 85 V
- [3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)



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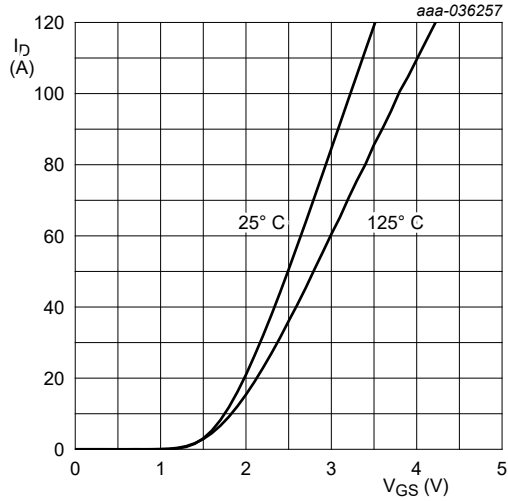
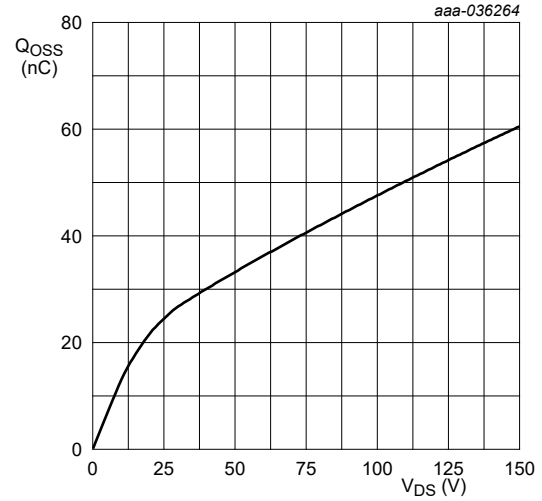
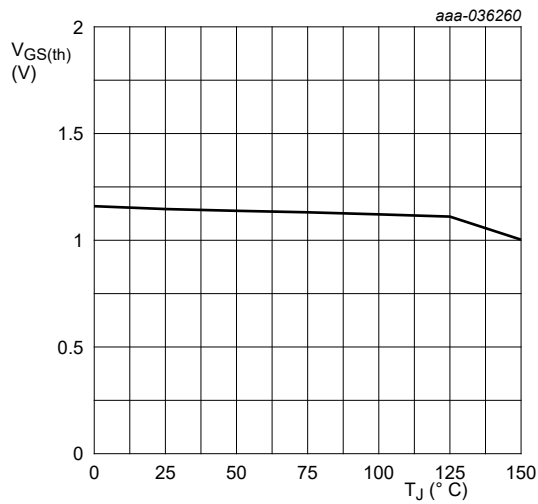


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values



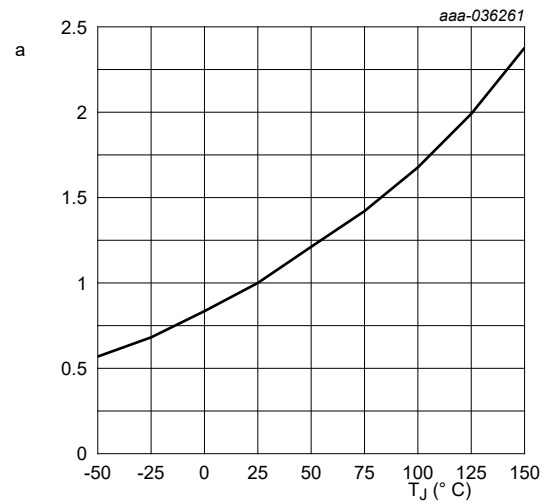
Freq. = 100 kHz

Fig. 7. Output charge as a function of drain-source voltage; typical values



$I_D = 5 \text{ mA}$; $V_{DS} = V_{GS}$

Fig. 8. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

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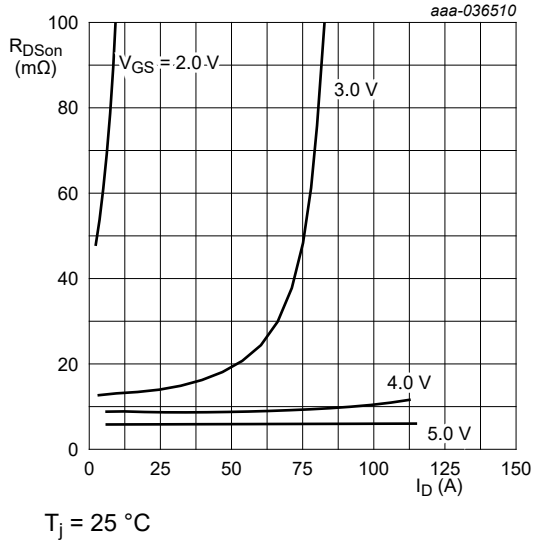


Fig. 10. Drain-source on-state resistance as a function of drain current ; typical values

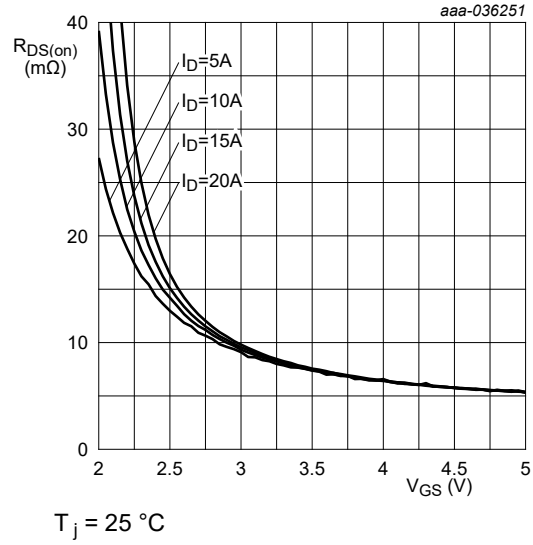


Fig. 11. Drain-source on-state resistance as a function of gate-source voltage; typical values

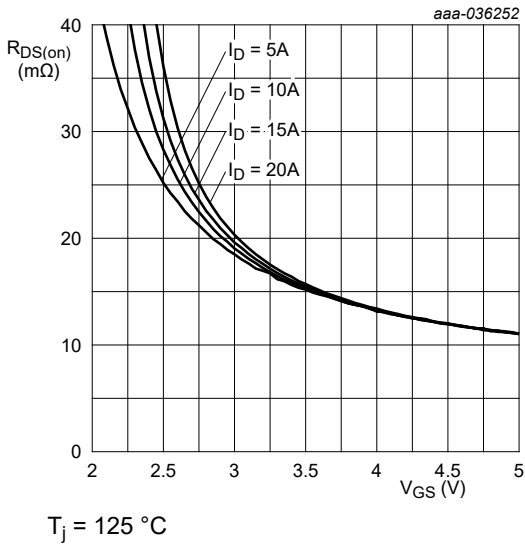


Fig. 12. Drain-source on-state resistance as a function of gate-source voltage; typical values

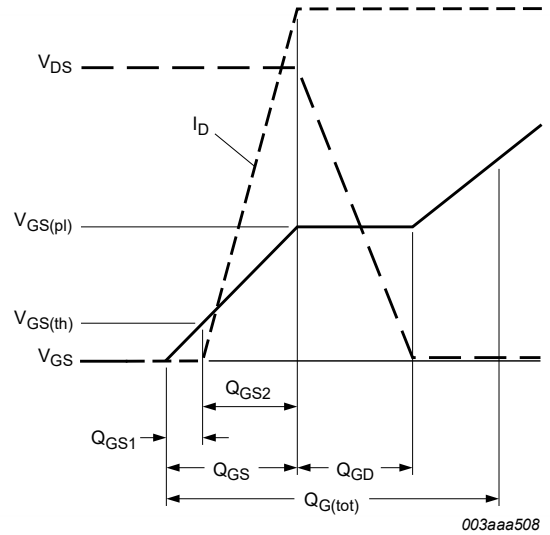
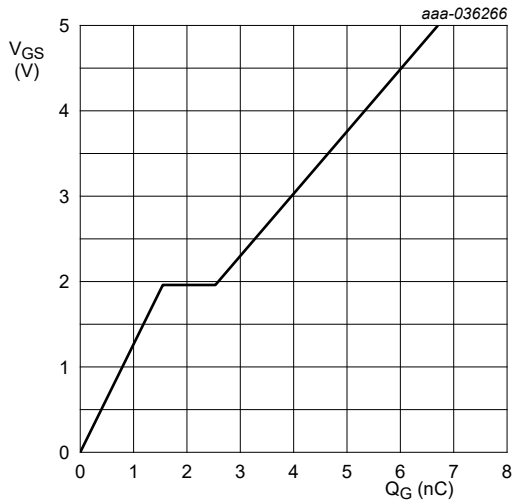


Fig. 13. Gate charge waveform definitions

150 V, 7 mOhm Gallium Nitride (GaN) FET in a 2.2 mm x 3.2 mm x 0.774 mm Land Grid Array (LGA) package



$T_J = 25\text{ }^\circ\text{C}$; $I_D = 10\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

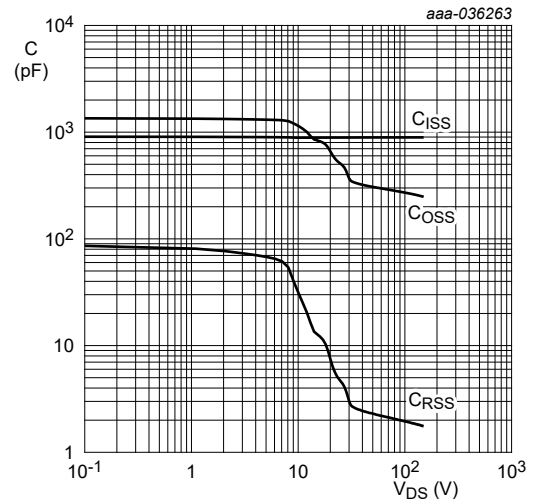
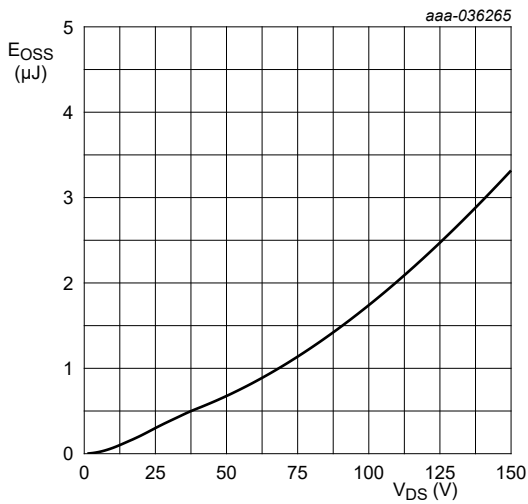
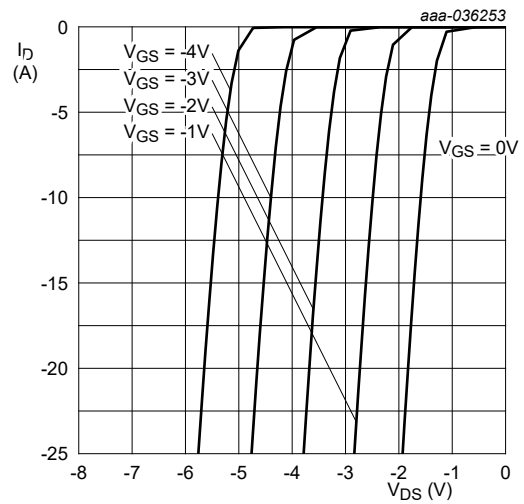


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

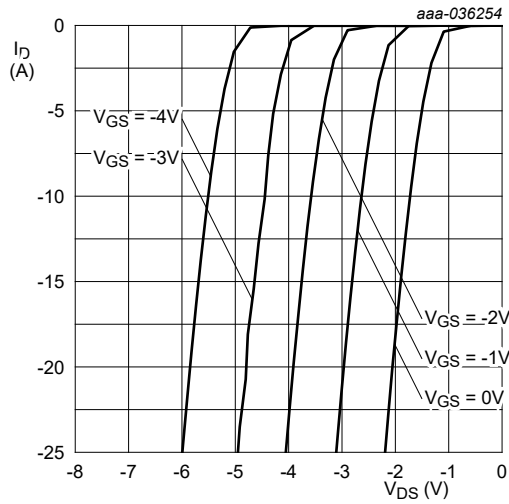
Fig. 16. COSS stored energy as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}$

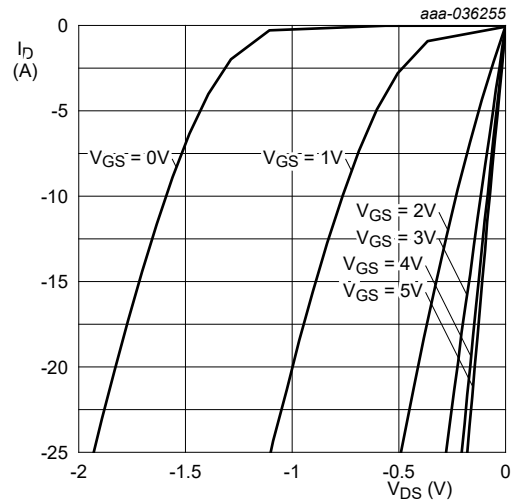
Fig. 17. Source current as a function of source-drain voltage; typical values

150 V, 7 mOhm Gallium Nitride (GaN) FET in a 2.2 mm x 3.2 mm x 0.774 mm Land Grid Array (LGA) package



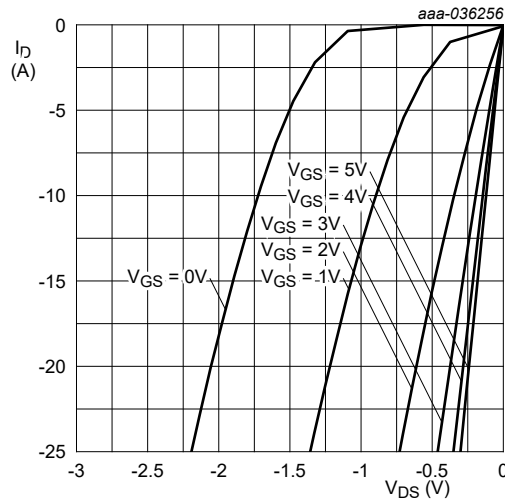
$T_j = 125\text{ °C}$

Fig. 18. Source current as a function of source-drain voltage; typical values



$T_j = 25\text{ °C}$

Fig. 19. Source current as a function of source-drain voltage; typical values



$T_j = 125\text{ °C}$

Fig. 20. Source current as a function of source-drain voltage; typical values

11. Package outline

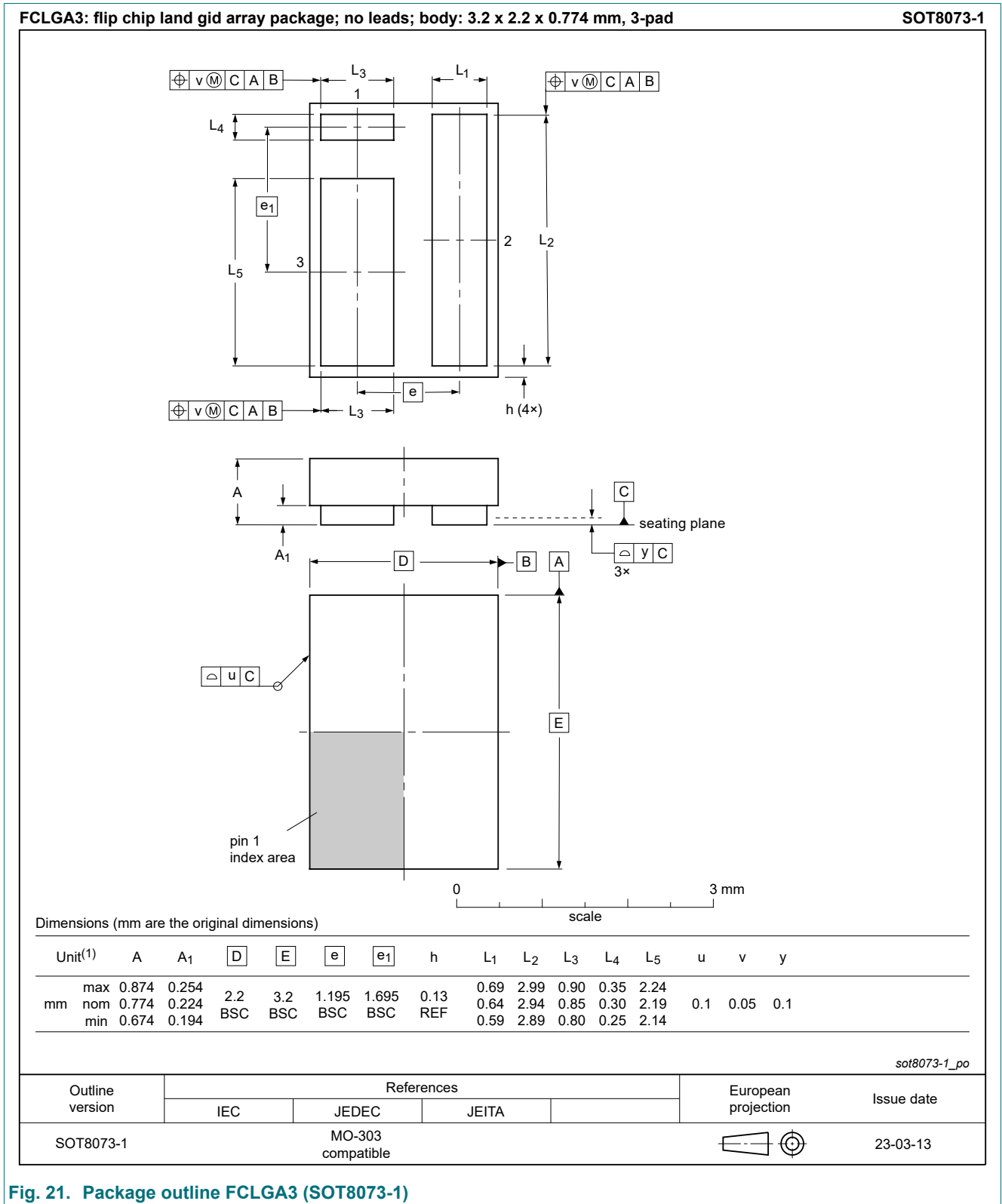


Fig. 21. Package outline FCLGA3 (SOT8073-1)

12. Soldering

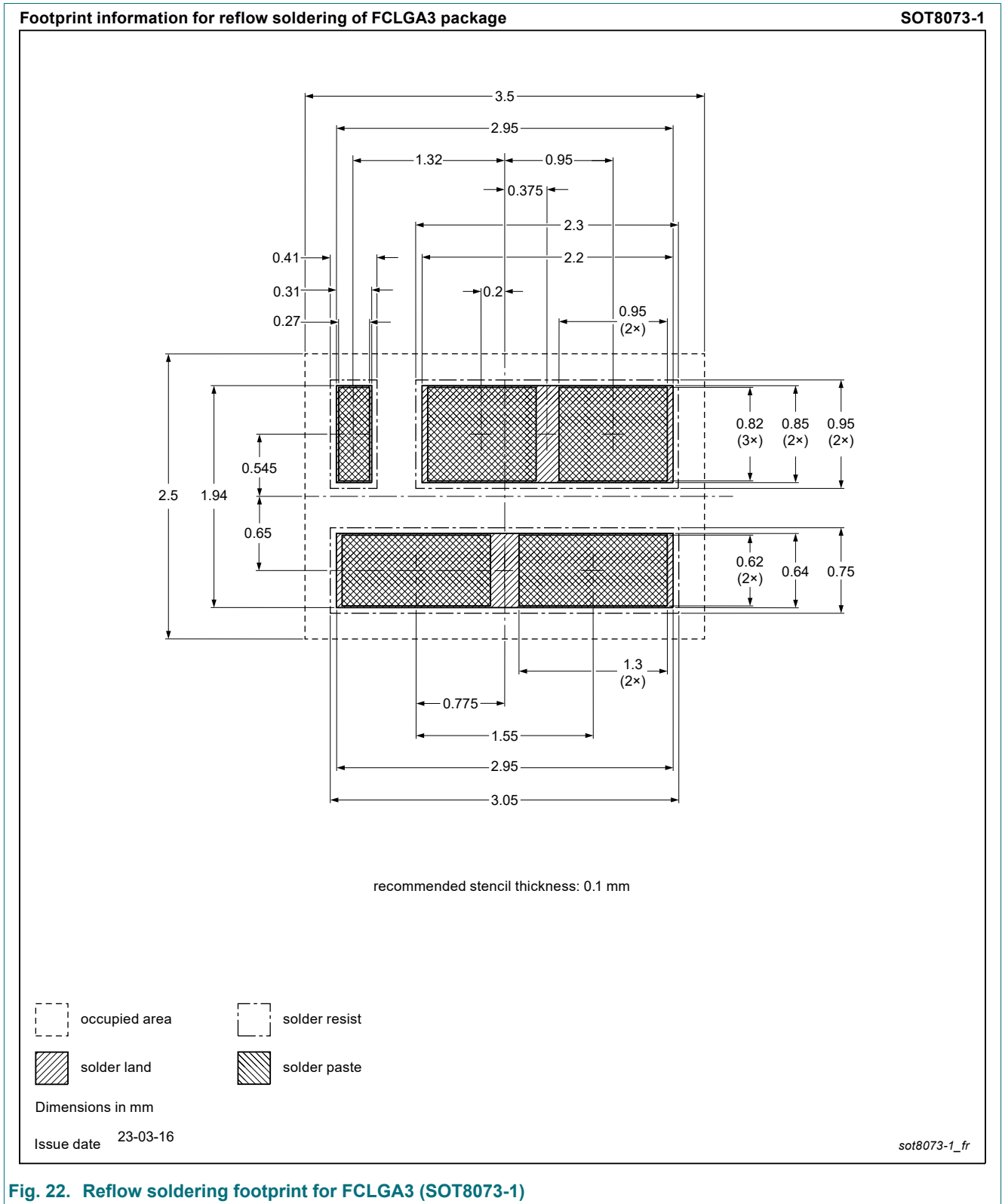


Fig. 22. Reflow soldering footprint for FCLGA3 (SOT8073-1)

150 V, 7 mOhm Gallium Nitride (GaN) FET in a 2.2 mm x 3.2 mm x 0.774 mm Land Grid Array (LGA) package

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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